IN THE CLAIMS

Please add claims 5-12 as follows

5. A system for overriding a signal during model simulation, said system comprising:

processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;

processing means for declaring a signal override during model simulation; and

processing means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means.

6. The system of claim 5, wherein said processing means for declaring a signal override further comprises processing means for instantiating an override enable port for delivering an override enable signal.

7. The system of claim 6, further comprising processing means for delivering said override enable signal from said override enable port to said signal selection means.

8. The system of claim 6, further comprising:

processing means for instantiating a latch that stores an override disable bit; and

processing means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection

means.

9. A computer program product for overriding a signal during model simulation, said computer program product comprising:

processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;

instruction means for declaring a signal override during model simulation; and

instruction means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means.

10. The computer program product of claim 9, wherein said instruction means for declaring a signal override further comprises instruction means for instantiating an override enable port for delivering an override enable signal.

11. The computer program product of claim 10, further comprising instruction means for delivering said override enable signal from said override enable port to said signal selection means.

12. The computer program product of claim 10, further comprising:

instruction means for instantiating a latch that stores an override disable bit; and

instruction means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection means.

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